

WE CLAIM:

1 1. An enhanced T-gate comprising:

2 a free T-gate, said free T-gate having a neck portion, said neck portion having a
3 height, and a T-bar portion, said T-bar portion having overhangs extending beyond said
4 neck portion by a first width; and

5 an insulator layer disposed on each side of said neck portion, forming a sandwich
6 structure with said neck portion along a width direction of said free T-gate, and wherein
7 said insulator layer only partially filling up a volume defined therebetween said overhangs
8 and a surface on which said free T-gate is standing.

1 2. The enhanced T-gate of claim 1, wherein in said sandwich structure said insulator layer
2 creating spacers on each side of said neck portion, wherein said spacers having a second
3 width, said second width being less than said first width of said overhangs, whereby that
4 part of said volume which is further from said neck portion than said second width is not
5 filled with said insulators.

1 3. The enhanced T-gate of claim 1, wherein in said sandwich structure said insulator layer
2 having approximately a C-shape, conformally adhering to a bottom surface of said
3 overhangs, to said neck portion, and to said surface on which said free T-gate is standing,
4 said insulator layer having a thickness which is less than half of said height of said neck

1 portion, wherein said insulator layer covering said surface on which said free T-gate is
2 standing and said bottom surface of said overhang to a distance from said neck portion
3 substantially equal to said first width, whereby that part of said volume which is inside
4 said C-shape is not filled by said insulator.

1 4. The enhanced T-gate of claim 1, wherein said insulator layer is a low-k material.

1 5. The enhanced T-gate of claim 4, wherein said low-k material is a compound of
2 materials selected from the group consisting of SiCO, SiCOH, SiCH, these silicon
3 containing materials with Si up to 100% replaced by Ge and these silicon containing
4 materials further containing atoms of materials selected from the group consisting of N
5 and F.

1 6. The enhanced T-gate of claim 4, wherein said low-k material is selected from the group
2 consisting of diamond-like carbon, fluorinated amorphous carbon, insulating inorganic
3 oxides, inorganic polymers, organic polymers, photosensitive organic materials,
4 fluorinated organic materials, other carbon-containing materials, hybrid organo-inorganic
5 materials and silsesquioxane-based materials.

1 7. A MODFET device comprising an enhanced T-gate, said enchanted T-gate further
2 comprising:

1 a free T-gate, said free T-gate having a neck portion and a T-bar portion, said T-
2 bar portion having overhangs extending beyond said neck portion; and
3 an insulator layer disposed on each side of said neck portion, forming a sandwich
4 structure with said neck portion along a width direction of said free T-gate, and wherein
5 said insulator layer only partially filling up a volume defined therebetween said overhangs
6 and a surface on which said free T-gate is standing.

1 8. The MODFET device of claim 7, further comprising a self-aligned source/drain
2 metallurgy, wherein a borderline of said metallurgy is defined by said insulator layer.
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1 9. An integrated circuit comprising at least one MODFET device, said MODFET device
2 comprising an enhanced T-gate, wherein said enhanced T-gate further comprising:

3 a free T-gate, said free T-gate having a neck portion and a T-bar portion, said T-
4 bar portion having overhangs extending beyond said neck portion; and

5 an insulator layer disposed on each side of said neck portion, forming a sandwich
6 structure with said neck portion along a width direction of said free T-gate, and wherein
7 said insulator layer only partially filling up a volume defined therebetween said overhangs
8 and a surface on which said free T-gate is standing.

1 10. The integrated circuit of claim 9, wherein said at least one MODFET further
2 comprising a self-aligned source/drain metallurgy, wherein a borderline of said

metallurgy is defined by said insulator layer.

11. The integrated circuit of claim 9, further comprising a multilevel interconnect structure of low-k interconnect dielectrics.

12. The integrated circuit of claim 11, wherein said low-k interconnect dielectrics leaving voids in said volume only partially filled up by said insulator layer.

13. The integrated circuit of claim 11, wherein said low-k interconnect dielectrics are materials selected from the group consisting of SiCO, SiCOH, SiCH, these silicon containing materials with Si up to 100% replaced by Ge, diamond-like carbon, fluorinated amorphous carbon, insulating inorganic oxides, inorganic polymers and organic polymers.

14. A method for producing an enhanced T-gate, comprising the steps of:

fabricating a free T-gate, said free T-gate having a neck portion and a T-bar portion;

coating conformally said free T-gate with an insulator; and

removing anisotropically said insulator by using said T-bar portion for masking, wherein leaving said insulator only underneath said T-bar portion, whereby said insulator forming sidewalls around said neck portion.

1 15. The method of claim 14, wherein the step of conformally coating further comprises
2 the step of adjusting a thickness of said insulator, wherein said thickness controls a width
3 of said sidewalls.

1 16. The method of claim 14, wherein the step of conformally coating is executed by
2 selecting a technique from the group consisting of: chemical vapor deposition (CVD),
3 plasma-enhanced CVD (PECVD), plasma polymerization, hot-filament-assisted CVD,
4 high-density-plasma PECVD, sputter deposition, reactive sputter deposition, ion beam
5 deposition, spinning from solution, spraying from solution and dipping.

1 17. The method of claim 14, wherein the step of anisotropically removing said insulator
2 further comprises the step of directionally etching said insulator.

1 18. The method of claim 14, wherein the step of anisotropically removing is executed
2 using reactive ion etching.

1 19. The method of claim 14, further comprising the steps of:
2 choosing for said insulator a positive-tone photosensitive material;
3 blanket exposing to light said positive-tone photosensitive material; and
4 developing said positive-tone photosensitive material,
5 whereby said positive-tone photosensitive material is readied for the step of removing

1 anisotropically.

1 20. The method of claim 14, wherein the step of anisotropically removing said insulator
2 further comprises the step of additional thinning said insulator underneath said T-bar
3 portion.

1 21. The method of claim 14, further comprising the step of employing low-k materials for
2 said insulator.

1 22. The method of claim 21, further comprising the step of choosing said low-k materials
2 from compounds of materials selected from the group consisting of SiCO, SiCOH, SiCH,
3 these silicon containing materials with Si up to 100% replaced by Ge and these silicon
4 containing materials further containing atoms of materials selected from the group
5 consisting of N and F.

1 23. The method of claim 21, further comprising the step of choosing said low-k materials
2 from materials selected from the group consisting of diamond-like carbon, fluorinated
3 amorphous carbon, insulating inorganic oxides, inorganic polymers, organic polymers,
4 photosensitive polymers, photosensitive polyimides and photosensitive amorphous
5 fluorocarbons.

1 24. A method for producing a high performance MODFET comprising an enhanced T-
2 gate, comprising the steps of:

3 fabricating a free T-gate, said free T-gate having a neck portion and a T-bar
4 portion;

5 coating conformally said free T-gate with an insulator;

6 removing anisotropically said insulator by using said T-bar portion for masking,
7 wherein leaving said insulator only underneath said T-bar portion; and

8 employing a self-aligned source/drain metallurgy, wherein said insulator forms a
9 borderline for said metallurgy.

1 25. The method of claim 24, further comprising the step of:

2 additional thinning of said insulator underneath said T-bar portion.

1 26. The method of claim 24, wherein the step of employing said self-aligned source/drain
2 metallurgy comprises the step of using angled deposition of a metal.

1 27. A method for manufacturing an integrated circuit comprising the steps of:

2 producing at least one high performance MODFET in said circuit, said step of
3 producing further comprising the steps of:

4 fabricating a free T-gate, said free T-gate having a neck portion and a T-bar
5 portion;

1 coating conformally said free T-gate with an insulator;
2 removing anisotropically said insulator by using said T-bar portion for masking,
3 wherein leaving said insulator only underneath said T-bar portion; and
4 employing a self-aligned source/drain metallurgy, wherein said insulator forms a
5 borderline for said metallurgy.

1 28. The method of claim 27, further comprising the step of:
2 depositing non-conformally an interconnect dielectric, whereby leaving gaps
3 underneath said T-bar portion.

1 29. The method of claim 27, further comprising the step of employing a multilevel
2 interconnect structure with low-k interconnect dielectrics.

1 30. The method of claim 29, further comprising the step of choosing said low-k
2 interconnect dielectrics from materials selected from the group consisting of SiCO,
3 SiCOH, SiCH, these silicon containing materials with Si up to 100% replaced by Ge,
4 diamond-like carbon, fluorinated amorphous carbon, insulating inorganic oxides,
5 inorganic polymers and organic polymers.